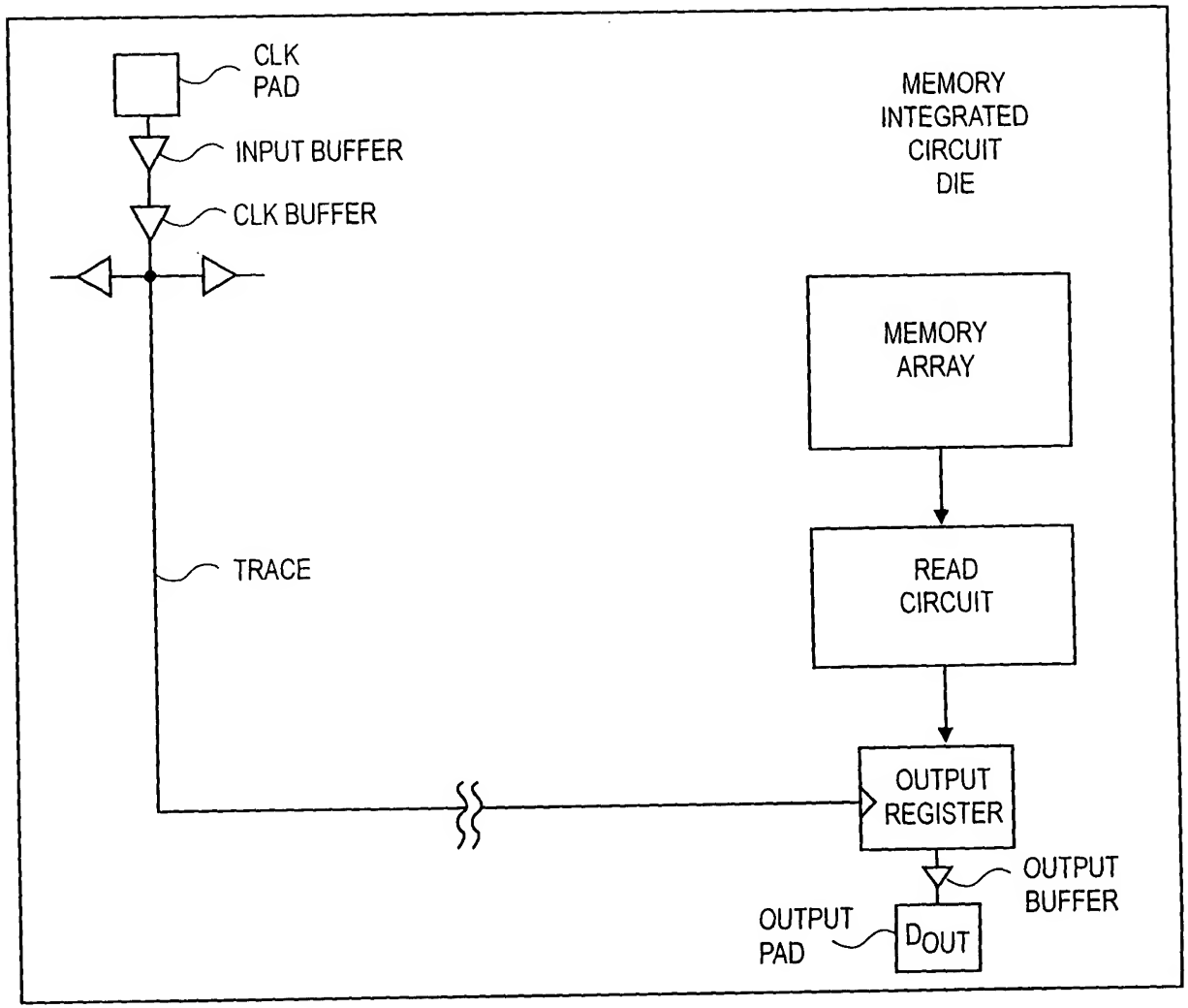
CLK
PAD
INPUT BUFFER
CLK BUFFER
MEMORY
INTEGRATED
CIRCUIT
DIE
MEMORY
ARRAY
TRACE
READ
CIRCUIT
OUTPUT
REGISTER
OUTPUT
BUFFER
OUTPUT
PAD
DOUT

FIG. 1A

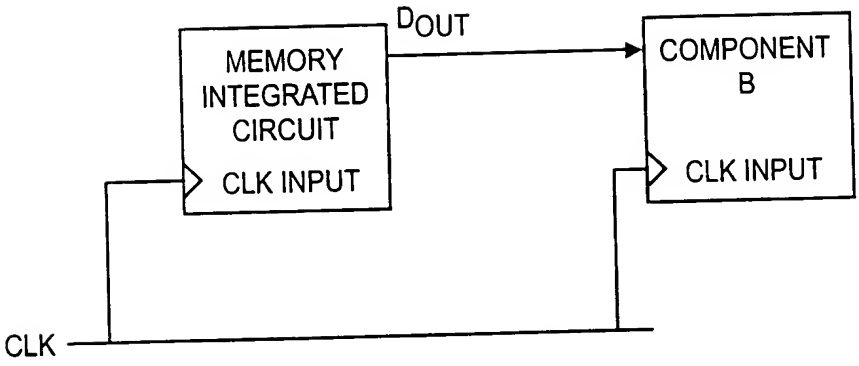
MEMORY
INTEGRATED
CIRCUIT
CLK INPUT
DOUT
COMPONENT
B
CLK INPUT
CLK

FIG. 1B

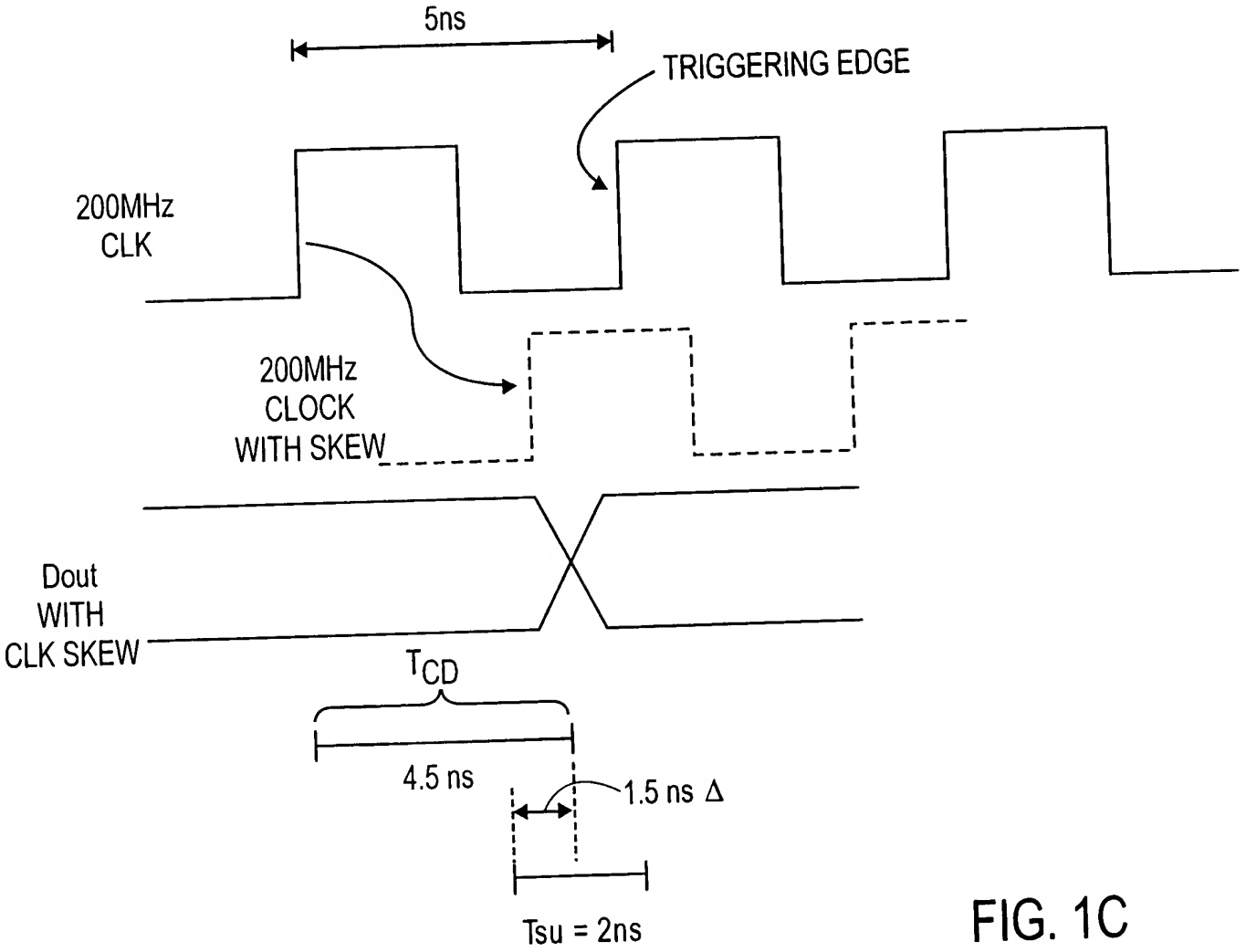
5ns
TRIGGERING EDGE
200MHz
CLK
200MHz
CLOCK
WITH SKEW
Dout
WITH
CLK SKEW
T_{CD}
4.5 ns
1.5 ns Δ
Tsu = 2ns

FIG. 1C

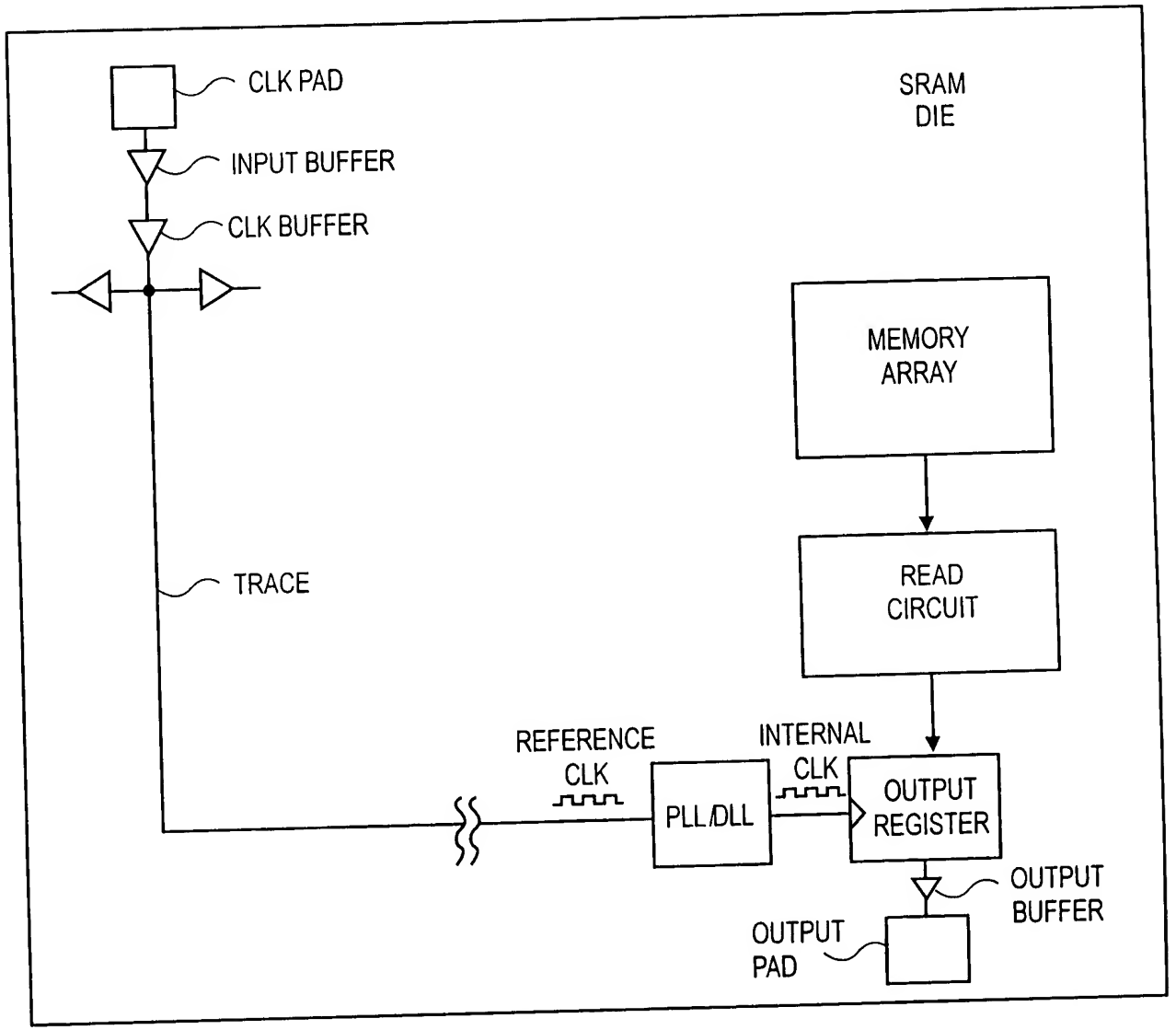
CLK PAD
SRAM
DIE
INPUT BUFFER
CLK BUFFER
MEMORY
ARRAY
TRACE
READ
CIRCUIT
REFERENCE
CLK
INTERNAL
CLK
PLL/DLL
OUTPUT
REGISTER
OUTPUT
BUFFER
OUTPUT
PAD

FIG. 2A

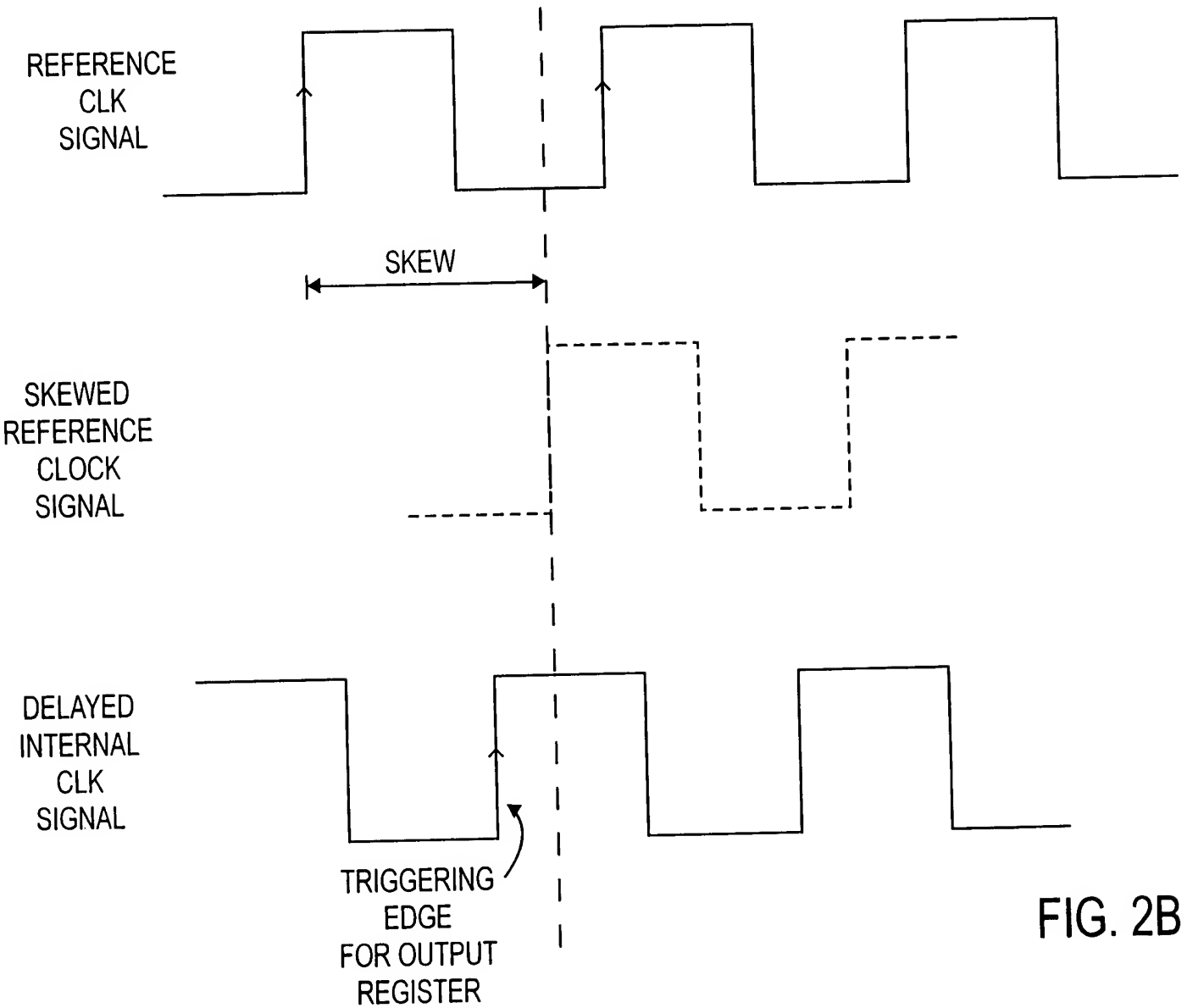
REFERENCE
CLK
SIGNAL
SKEW
SKEWED
REFERENCE
CLOCK
SIGNAL
DELAYED
INTERNAL
CLK
SIGNAL
TRIGGERING
EDGE
FOR OUTPUT
REGISTER

FIG. 2B

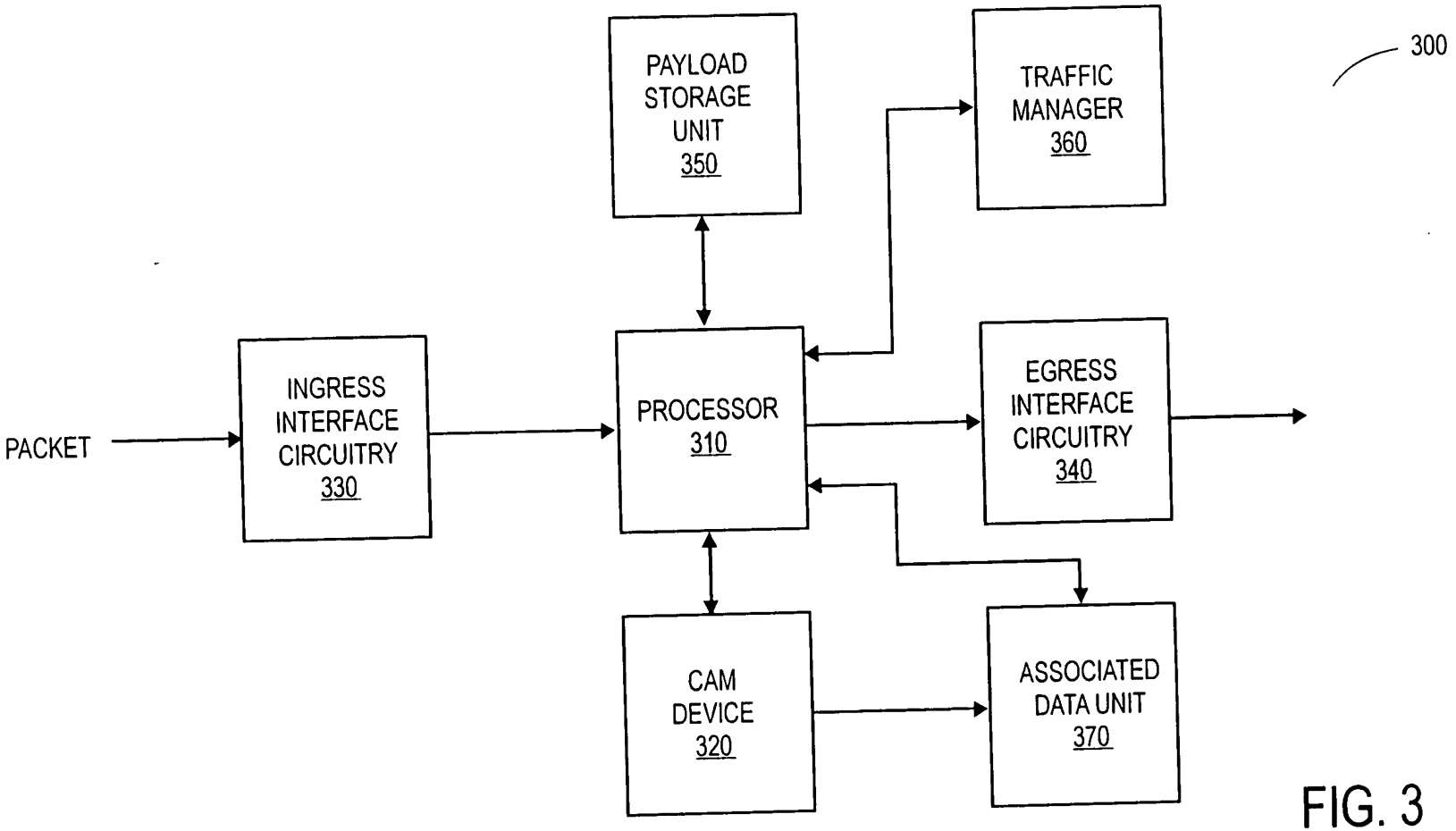
300
PAYLOAD STORAGE UNIT 350
TRAFFIC MANAGER 360
PACKET
INGRESS INTERFACE CIRCUITRY 330
PROCESSOR 310
EGRESS INTERFACE CIRCUITRY 340
CAM DEVICE 320
ASSOCIATED DATA UNIT 370

FIG. 3

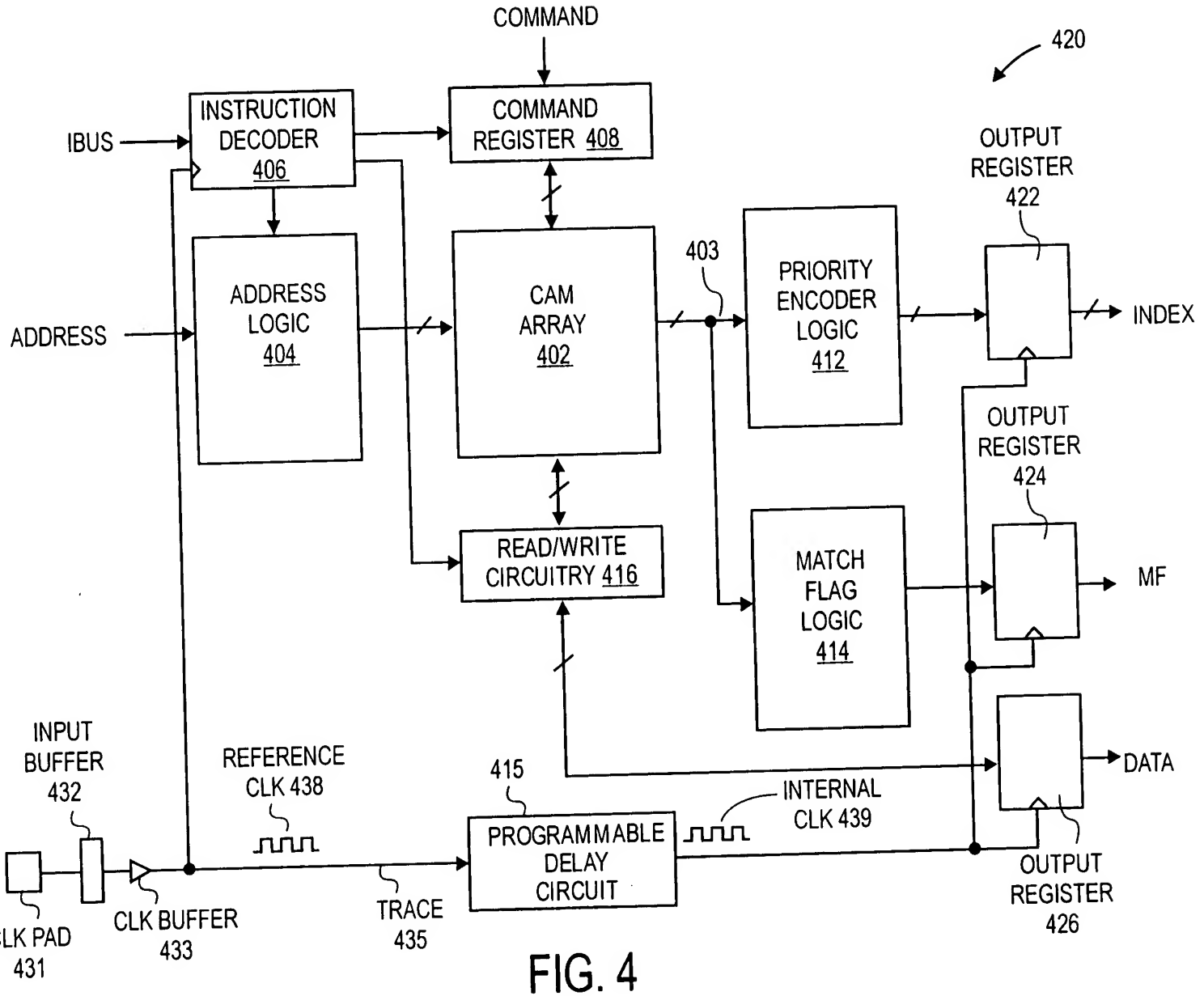
COMMAND
420
INSTRUCTION DECODER 406
IBUS
COMMAND REGISTER 408
OUTPUT REGISTER 422
ADDRESS
ADDRESS LOGIC 404
CAM ARRAY 402
403
PRIORITY ENCODER LOGIC 412
INDEX
OUTPUT REGISTER 424
READ/WRITE CIRCUITRY 416
MATCH FLAG LOGIC 414
MF
INPUT BUFFER 432
REFERENCE CLK 438
415
INTERNAL CLK 439
DATA
PROGRAMMABLE DELAY CIRCUIT
CLK PAD 431
CLK BUFFER 433
TRACE 435
OUTPUT REGISTER 426

FIG. 4

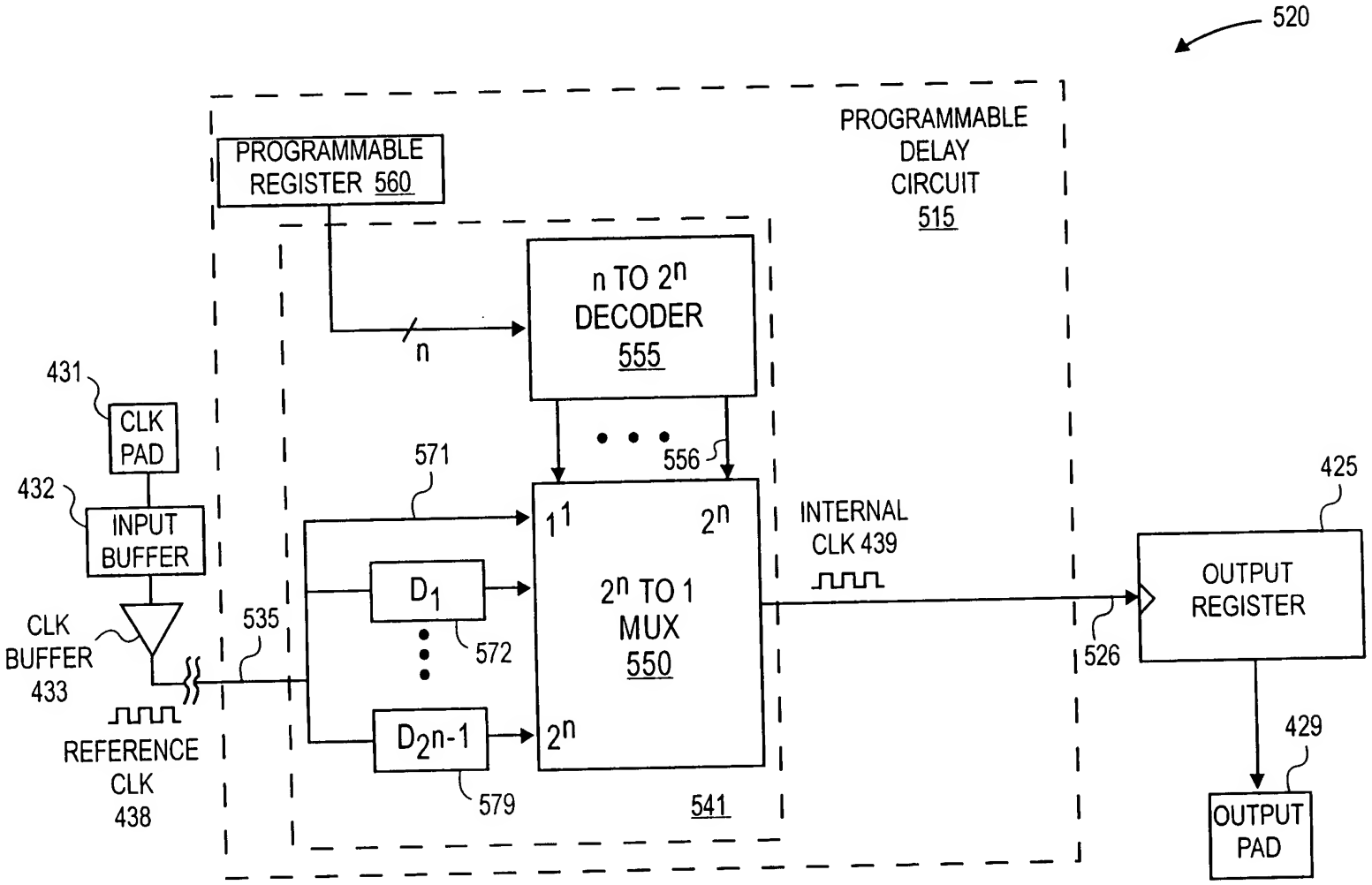
520
PROGRAMMABLE DELAY CIRCUIT 515
PROGRAMMABLE REGISTER 560
n TO 2n DECODER 555
n
431
CLK PAD
432
INPUT BUFFER
CLK BUFFER 433
REFERENCE CLK 438
535
571
556
D1
D2n-1
572
579
1
2n
2n TO 1 MUX 550
541
INTERNAL CLK 439
526
425
OUTPUT REGISTER
429
OUTPUT PAD

FIG. 5A

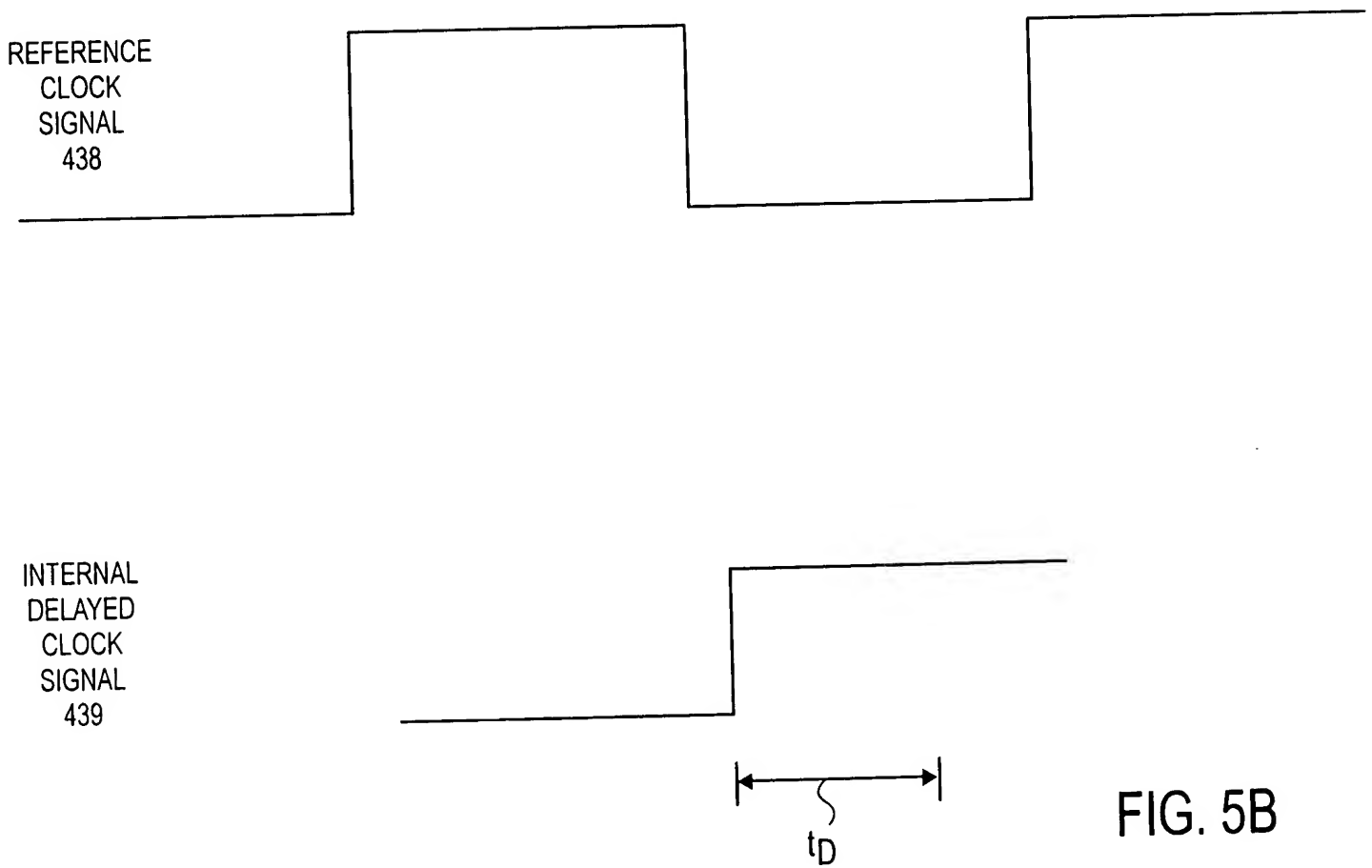
REFERENCE
CLOCK
SIGNAL
438
INTERNAL
DELAYED
CLOCK
SIGNAL
439
t_D

FIG. 5B

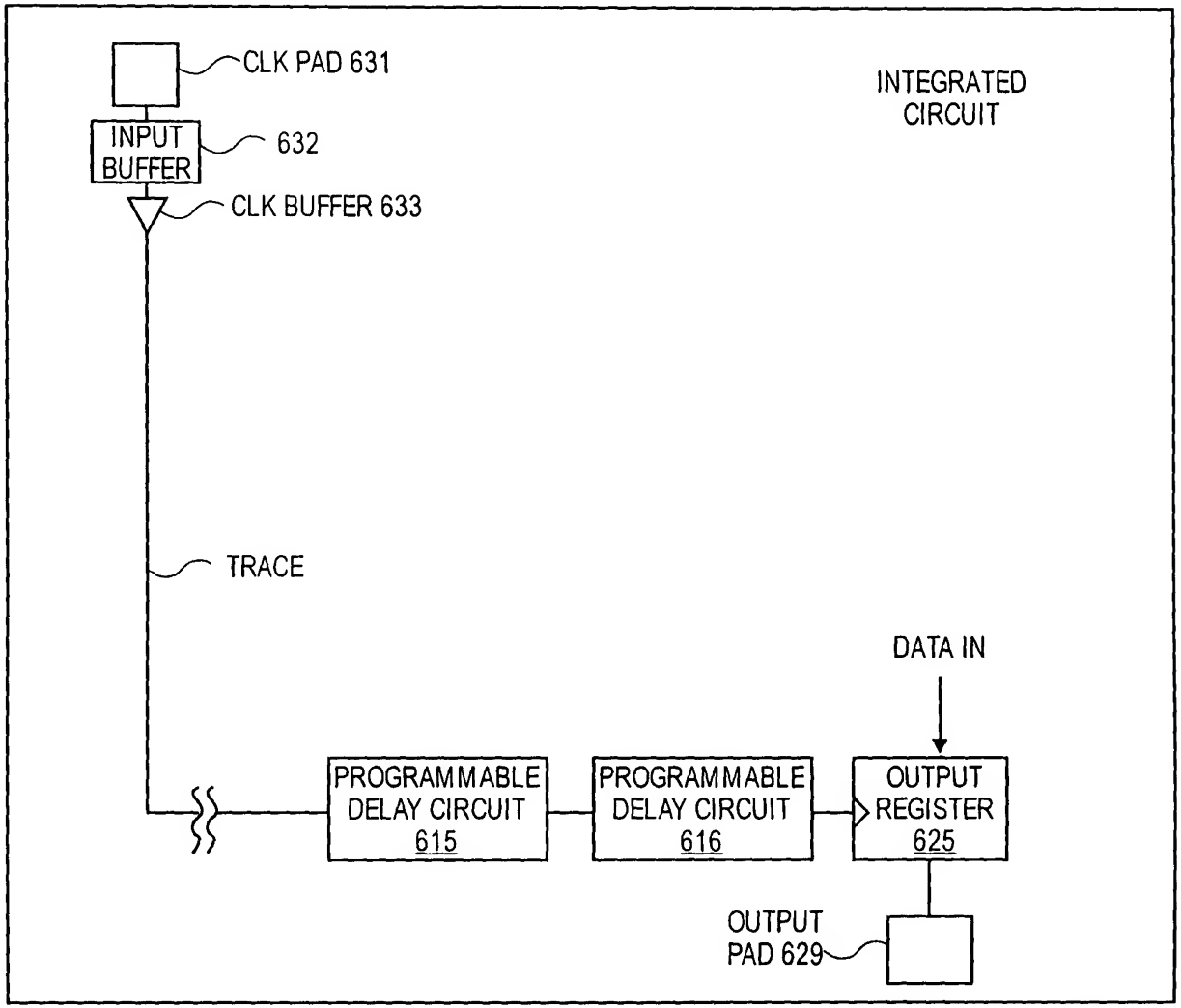
CLK PAD 631
INTEGRATED CIRCUIT
INPUT BUFFER
632
CLK BUFFER 633
TRACE
DATA IN
PROGRAMMABLE DELAY CIRCUIT 615
PROGRAMMABLE DELAY CIRCUIT 616
OUTPUT REGISTER 625
OUTPUT PAD 629

FIG. 6

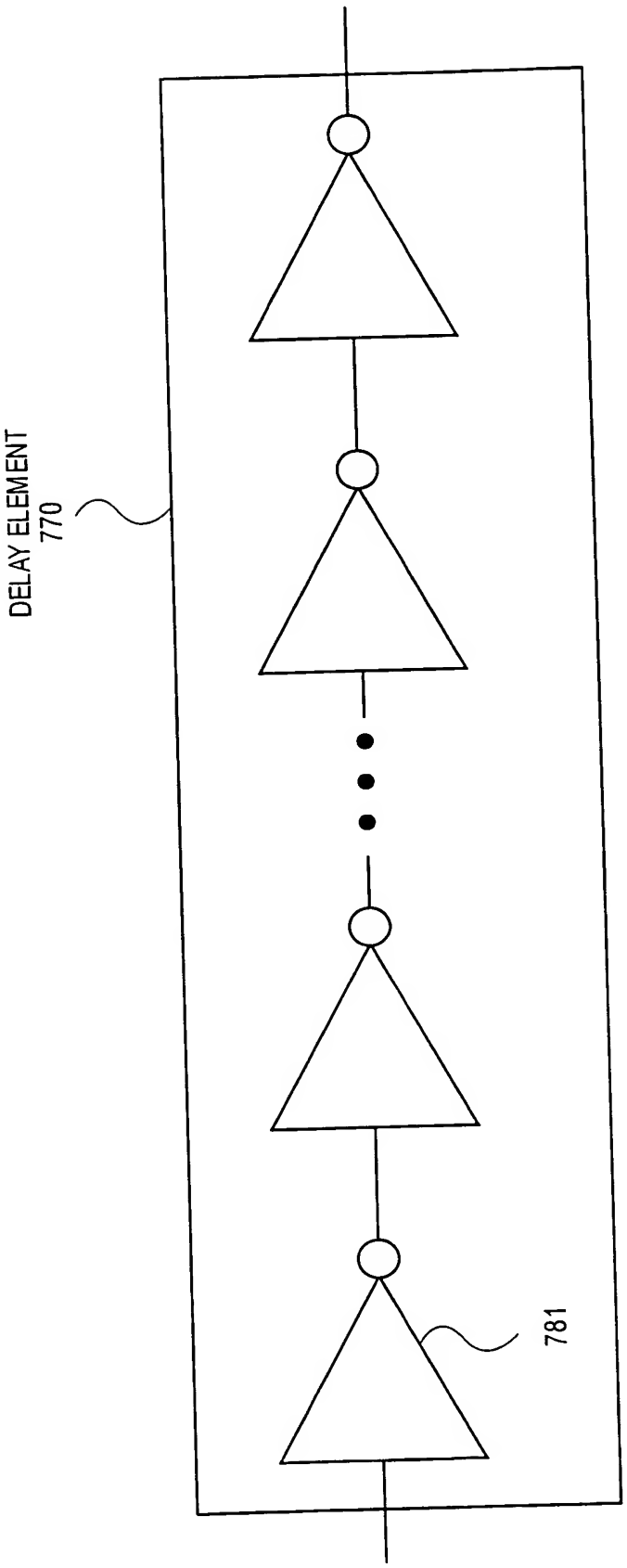

FIG. 7

REFERENCE CLOCK SIGNAL FREQUENCY RANGE	PROGRAMMABLE REGISTER BIT VALUES	DELAY ELEMENT	DELAY VALUE
200 MHZ	0 0 0 0	D_2^n-1	3ns
250 MHZ	0 0 0 1	D_2^n-2	2ns
333 MHZ	0 0 1 0	D_2^n-3	1ns
• • •	• • •	• • •	• • •
400 MHZ	1 1 1 1	—	0ns

FIG. 8

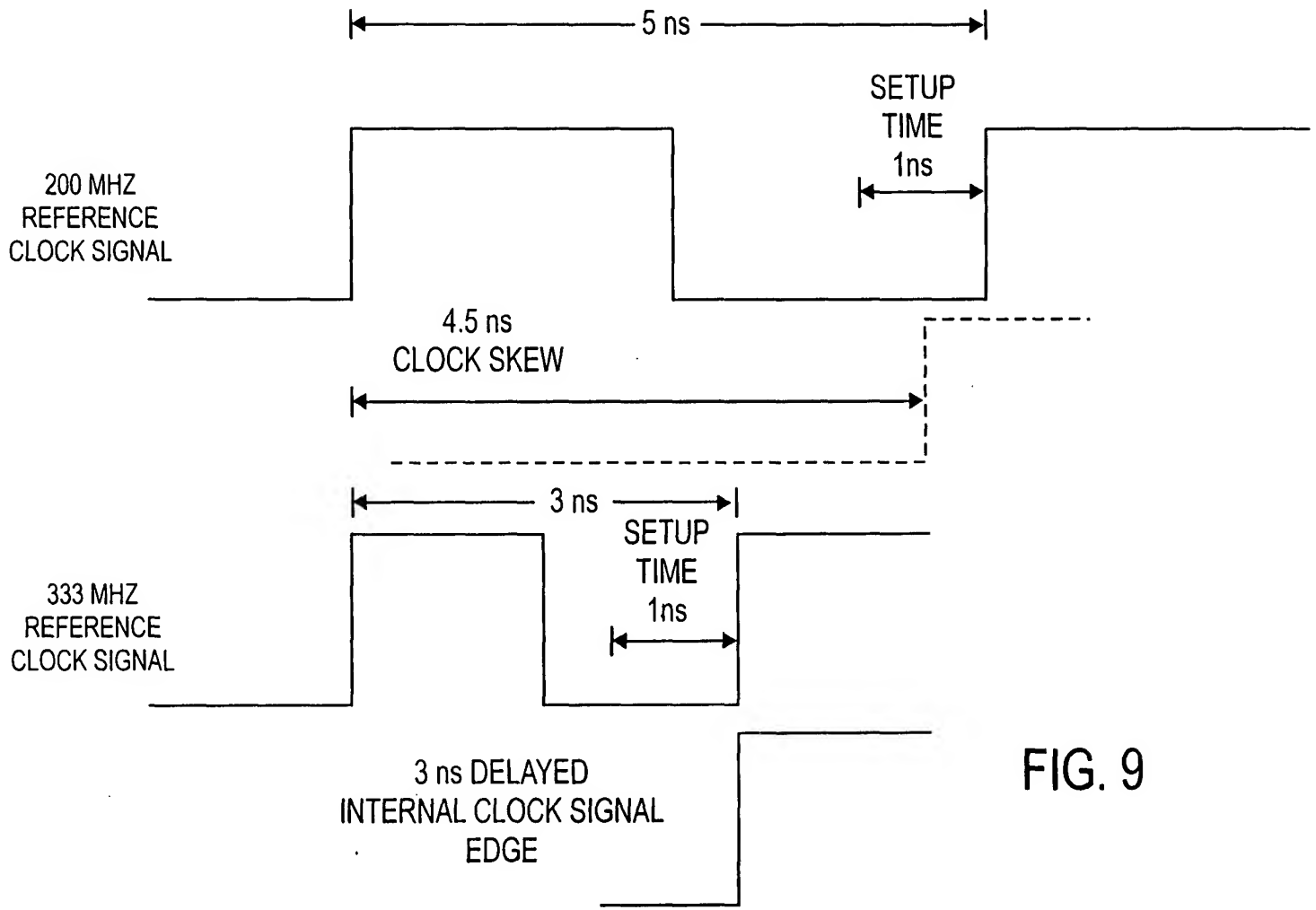
5 ns
SETUP
TIME
1ns
200 MHZ
REFERENCE
CLOCK SIGNAL
4.5 ns
CLOCK SKEW
3 ns
SETUP
TIME
1ns
333 MHZ
REFERENCE
CLOCK SIGNAL
3 ns DELAYED
INTERNAL CLOCK SIGNAL
EDGE

FIG. 9